**In the Claims:**

1. (Currently Amended) ~~Process~~A method for the verification of digital circuits, wherein a digital circuit ~~(6)~~ to be verified is compared with a reference description ~~(5)~~ of the digital circuit, in order through an equivalence test to recognize errors in the digital circuit,

~~characterised in~~wherein

(a) ~~that~~ for specific circuit structures described by the reference description ~~(5)~~ of the digital circuit, for which different implementation alternatives ~~(7)~~ are known, in each case ~~that~~ an implementation alternative that ~~(7), which~~ has the greatest degree of structural equivalence with the digital circuit ~~(6)~~ to be verified, is determined, whereby the different implementation alternatives are simulated respectively in combination with the reference description and compared with a corresponding simulation of the digital circuit, in order to determine as the implementation alternative with the greatest degree of structural equivalence with the digital circuit, the implementation alternative, which in this case for several simulation patterns has the greatest equivalence of design points with the digital circuit,

(b) ~~that~~ in the reference description ~~(5)~~ of the digital circuit, the description of the individual circuit structures is replaced by the implementation alternative ~~(7)~~ determined for the respective circuit structure in step (a) with the greatest degree of structural equivalence in each case, and

(c) ~~that~~ the equivalence test is executed by comparing the digital circuit ~~(6)~~ with the reference description ~~(5)~~ changed in accordance with step (b).

2. (Currently Amended) ~~Process~~The method according to Claim 1, ~~characterised in that~~wherein the specific circuit structures, for which in step (a) the implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures.

3. (Currently Amended) ~~Process~~The method according to Claim 2, ~~characterised in that~~wherein the specific circuit structures, for which in step (a) the implementation alternative ~~(7)~~ with the greatest degree of equivalence

is determined in each case, are multiplier structures for realizing integral multiplication functions.

4. (Currently Amended) ~~Process~~The method according to ~~any one of the preceding claims, characterised in that~~claim 1, wherein the ~~process~~method is executed computer-aided.

5. (Currently Amended) ~~Process~~The method according to ~~any one of the preceding claims, characterised in that~~ claim 1, wherein the reference description ~~(5)~~ is selected from a group comprising RTL-, VHDL- and Verilog-descriptions.

6. (Currently Amended) ~~Process~~The method according to ~~any one of the preceding claims, characterised in that~~ claim 1, wherein in step (c) the equivalence test is executed by comparing an existing implementation of the digital circuit ~~(6)~~ with the reference description ~~(5)~~ changed in step (b).

7. (Currently Amended) ~~Process~~The method according to ~~any one of the preceding claims, characterised in that~~ claim 1, wherein the pre-defined implementation alternatives ~~(7)~~ for the specific circuit structures comprise varying architectures of ~~these~~the specific circuit structures aided by a synthesis device available for the design of the digital circuit.

8. (Cancelled)

9. (Currently Amended) ~~Process~~The method according to Claim ~~8~~1, ~~characterised in that~~wherein in step (a) for each circuit structure, the different implementation alternatives ~~(7)~~ are simulated at the same time and compared with the simulation of the digital circuit ~~(6)~~.

10. (Currently Amended) ~~Process~~The method according to Claim 9, ~~characterised in that~~wherein the different implementation alternatives ~~(7)~~ for each circuit structure are simulated at the same time by inputs of the implementation alternatives ~~(7)~~ being connected with one another and corresponding outputs of the implementation alternatives ~~(7)~~ being led to a

common output ~~so maintaining~~ to maintain the circuit function of the individual implementation alternatives.

11. (Currently Amended) ~~Process~~The method according to Claim 10, ~~characterised in that~~wherein the outputs of the different implementation alternatives ~~(7)~~ are connected by a logic OR link to the common output.

12. (Currently Amended) ~~Process~~The method according to ~~any one of~~ Claims ~~8-11~~, ~~characterised in that~~wherein for each implementation alternative ~~(7)~~ in step (a), the degree of equivalence with the simulation of the digital circuit ~~(6)~~ is obtained by the number of ~~the~~ values output for ~~the~~ individual simulation patterns of the reference description ~~(5)~~ with the respective implementation alternative, the alternative values identically output, which are identical to ~~the~~ values output by the digital circuit ~~(6)~~ for the corresponding simulation patterns, being determined for the ~~several~~ simulation patterns for each implementation alternative ~~(7)~~ and being used as degree of equivalence for the corresponding implementation alternative ~~(7)~~.

13. (Currently Amended) ~~Process~~The method according to ~~any one of the preceding claims, characterised in that a process~~Claim 1, wherein a method of equivalence class refinement is used for determining the implementation alternatives ~~(7)~~ with the greatest degree of structural equivalence carried out in step (a).

14. (Currently Amended) ~~Device~~A device for the verification of digital circuits,

with first memory means ~~(6)~~ for storing a description of a digital circuit to be verified,

with second memory means ~~(5)~~ for storing a reference description of the digital circuit, and

with verification means ~~(2)~~, which are set up in such a manner that ~~they~~ the verification means compare the description of the digital circuit ~~(6)~~ to be verified with the reference description ~~(5)~~, in order through an equivalence test to recognize errors in the digital circuit,

~~characterised in~~wherein

~~that~~ third memory means ~~(7)~~ are provided for storing different pre-defined implementation alternatives for specific circuit structures of the digital circuit, whereby the verification means are set up in such a manner that, for the specific circuit structures in each case, the verification means determine an implementation alternative that has the greatest degree of structural equivalence with the digital circuit to be verified,

~~that~~ the verification means ~~(2)~~ are set up in such a manner that for the specific circuit structures in each case the verification means ~~they~~ determine ~~that~~ an implementation alternative, which has the greatest degree of structural equivalence with the digital circuit to be verified,

the verification means are set up in such a manner that, for determining the implementation alternative with the greatest degree of structural equivalence with the digital circuit in each case, the verification means simulate the different implementation alternatives respectively in combination with the reference description and compare the simulations with a corresponding simulation of the digital circuit, to determine the implementation alternative with the greatest degree of structural equivalence with the digital circuit, which for simulation patterns has the greatest equivalence of design points with the digital circuit, and

~~that~~ the verification means ~~(2)~~ are set up in such a manner that the verification means ~~they~~ insert the previously determined implementation alternatives with the greatest degree of structural equivalence respectively in the reference description of the digital circuit for the individual specific circuit structures and compare the description of the digital circuit to be verified with the reference description thus changed for executing the equivalence test.

15. (Currently Amended) ~~Device~~The device according to Claim 14, ~~characterised in that~~wherein the device is set up to execute the ~~process~~method according to Claim 1~~any one of Claims 1-13~~.

16. (Currently Amended) ~~Computer~~A computer-program product with a program-code stored on a data medium ~~(3)~~, for executing the ~~process~~method according to Claim 1~~any one of Claims 1-13~~, whenever the program-code is run in a computer system ~~(1)~~.

17. (Currently Amended) ~~Digital~~ A digital storage medium ~~(3)~~ with electronically readable control signals, which can cooperate with a computer system, so that the ~~process~~method is executed according to Claim 1~~any one of Claims 1-13~~.